IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Nicholas Oleksinski et al.
Serial No.:	10/602,937
Title:	TIMING CONSTRAINT GENERATOR
Filed:	June 24, 2003
Attorney Docket No.:	1496.00302
Examiner:	Tat, B.
Art Unit:	2825

CERTIFICATE OF MAILING

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 19, 2005.

By: Jan M. Dunbar
Jan M. Dunbar

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal by an attorney either of record or acting under 37 CFR 1.34.

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REMARKS

Review is requested for the following reasons:

1. The Examiner has omitted one or more elements needed to make a *prima facie* rejection.

The Examiner has omitted evidence against claim 7 in the rejection and thus has failed to establish *prima facie* anticipation under 35 U.S.C. §102. Claim 7 is rejected under Batchelor, U.S. Publication 2004/0025129. However, the cites in the Office Action are actually to U.S. Patent No. 5,825,658 to Ginetti et al. which is not in the basis for rejection. See the arguments in the Response After Final, page 24 lines 3-14.

The Examiner has omitted the structure of claims 21 and 22 in the rejections and thus has failed to establish *prima facie* anticipation under 35 U.S.C. §102. Both claims 20 and 21 provide a medium and a computer program recorded in the medium. The rejection of claims 20 and 21 on page 2 of the Office Action do not address either element. See the arguments in the Response After Final, page 17 lines 6-14.

2. Multiple claim limitation are not met by the reference.

Batchelor does not describe every limitation of claim 1 step (A) , claim 14 step (A), claim 20 step (A) and claim 21 step (A) and thus does not anticipate under 35 U.S.C. §102. In particular, Batchelor is silent regarding a step for identifying a plurality of clock signals by analyzing a circuit design as

claimed. See the arguments in the Response After Final, page 12 line 4 through page 13 line 8.

Batchelor does not describe every limitation of claim 1 step (B) and claim 20 step (B) and thus does not anticipate under 35 U.S.C. §102. In particular, Batchelor is silent regarding a step for determining a plurality of relationships among the plurality of clock signals as claimed. See the arguments in the Response After Final, page 13 line 9 through page 15 line 29.

Batchelor does not describe every limitation of claim 1 step (C) and claim 20 step (C) and thus does not anticipate under 35 U.S.C. §102. In particular, Batchelor is silent regarding a step for generating the plurality of timing constraints for the circuit design in response to the plurality of clock signals and the plurality of relationships as claimed. See the arguments in the Response After Final, page 15 line 30 through page 17 line 5.

Batchelor does not describe every limitation of claim 14 step (B) and claim 21 step (B) and thus does not anticipate under 35 U.S.C. §102. In particular, Batchelor is silent regarding a step for querying a user for a plurality of parameters for the plurality of clock signals as claimed. See the arguments in the Response After Final, page 18 lines 4-17.

Batchelor does not describe every limitation of claim 14 step (C) and claim 21 step (C) and thus does not anticipate under 35 U.S.C. §102. In particular, Batchelor is silent regarding a step for generating the plurality of timing constraints in response to the plurality of clock signals and the plurality of parameters.

See the arguments in the Response After Final, page 18 line 18 through page 19 line 10.

Batchelor does not describe every limitation of claim 2 and thus does not anticipate under 35 U.S.C. §102. Claim 2 provides that the plurality of clock signals comprise a test clock signal. In contrast, none of the clock signals of Batchelor are described as test clock signals. Furthermore, the Examiner has not identified a clock signal of Batchelor that one of ordinary skill in the art would consider to be similar to the claimed test clock signal. See the arguments in the Response After Final, page 19 line 20 through page 20 line 25.

Batchelor does not describe every limitation of claim 12 and thus does not anticipate under 35 U.S.C. §102. Batchelor is silent regarding a sub-step for generating a shared structure relationship of the plurality of relationships between a test clock signal of the plurality of clock signals and a normal clock signal of the clock signals, each driving a particular structure of the circuit design in different modes for the circuit design as claimed. See the arguments in the Response After Final, page 27 line 7 through page 28 line 2.

Applicants' representative believes that the Examiner has omitted one or more essential elements needed for a *prima facie* anticipation rejection. Furthermore, Batchelor does not expressly or inherently disclose all of the elements and limitations as arranged in the claims. As such, the review panel is respectfully requested to either (i) allow the application or (ii) withdraw the

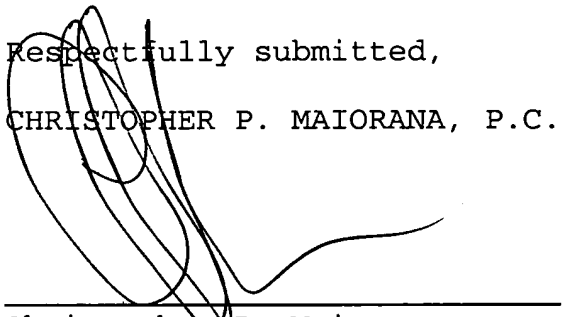
finality of the April 20, 2005 Office Action and return the application to prosecution.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Dated: August 19, 2005

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Docket No.: 03-0228 / 1496.00302